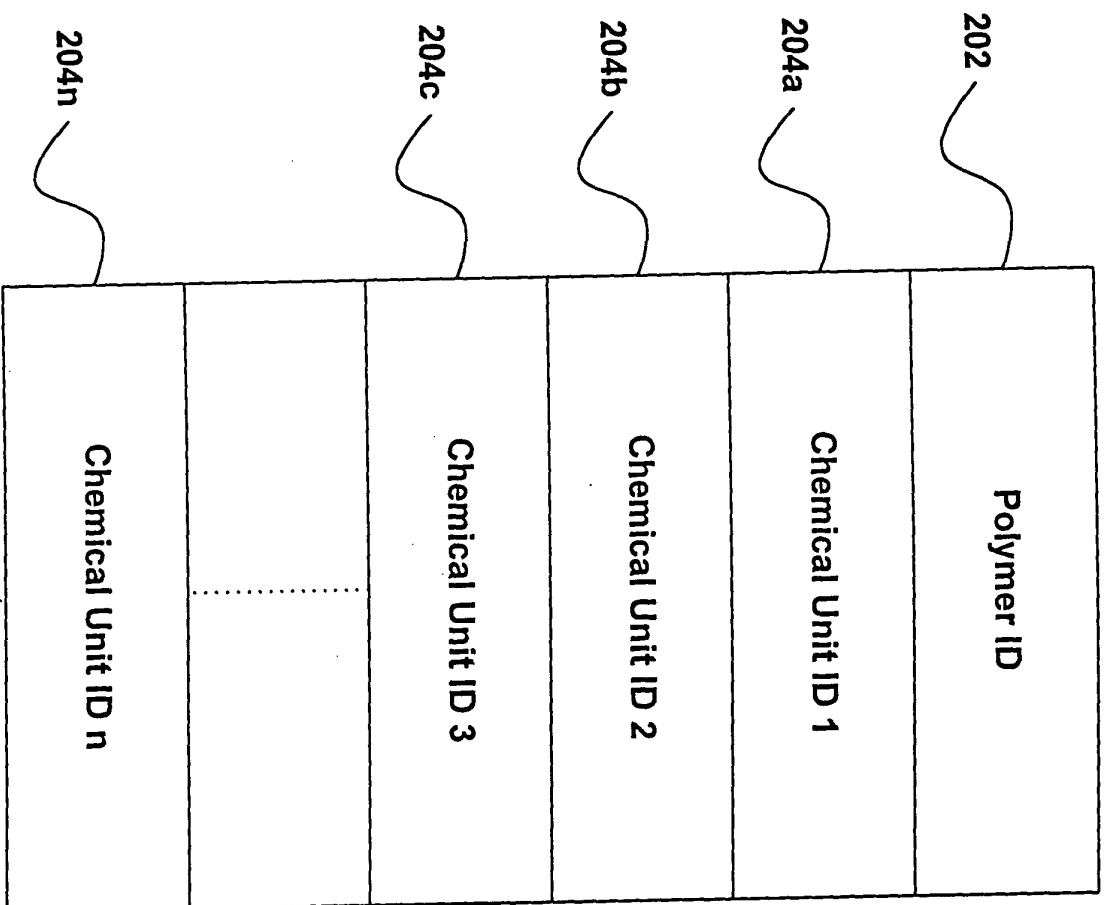


FIG. 1



200

FIG. 2A

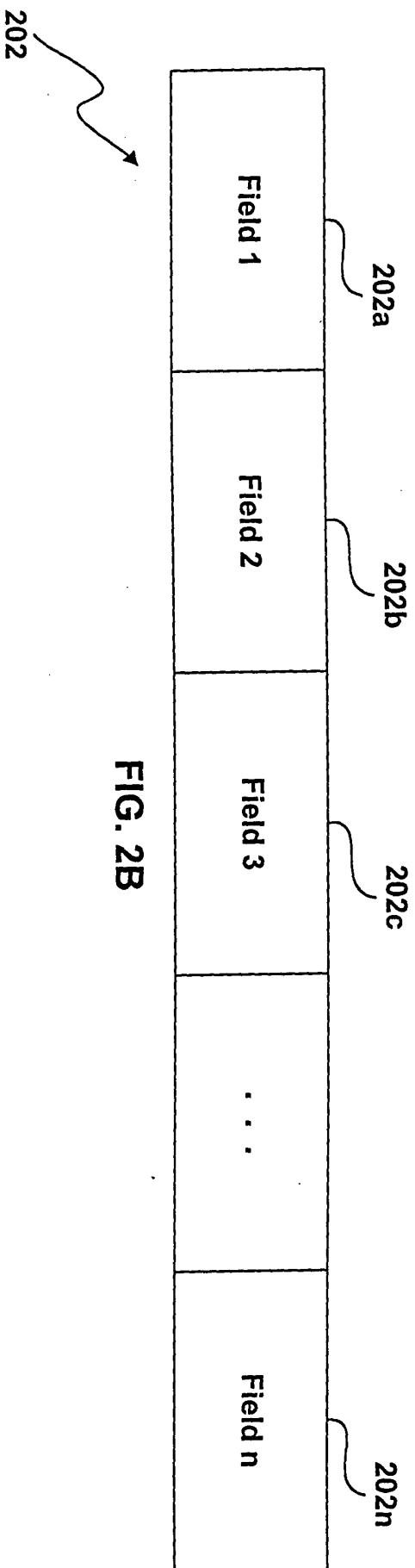


FIG. 2B

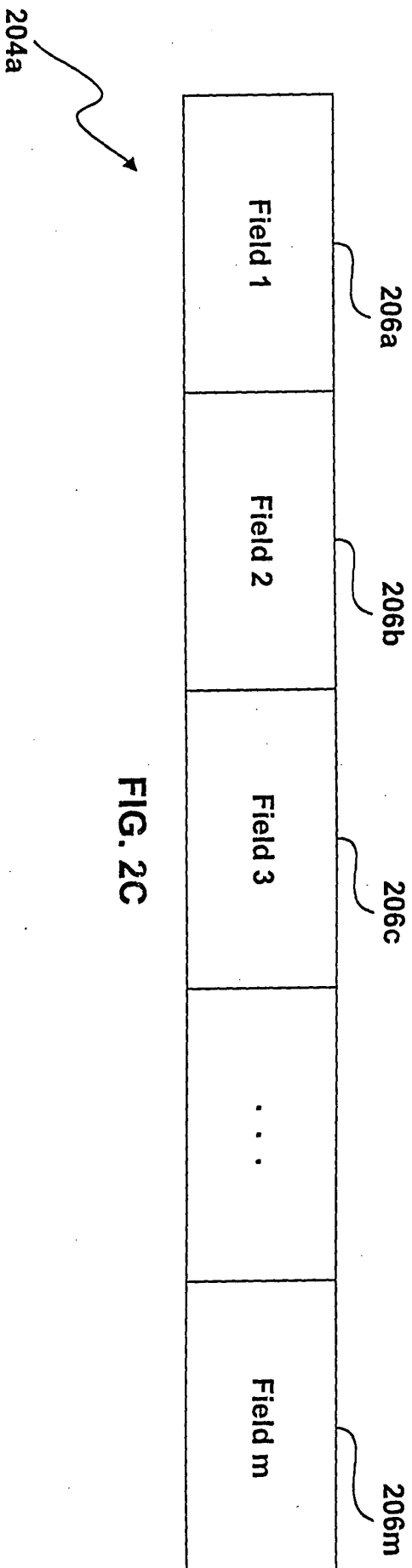
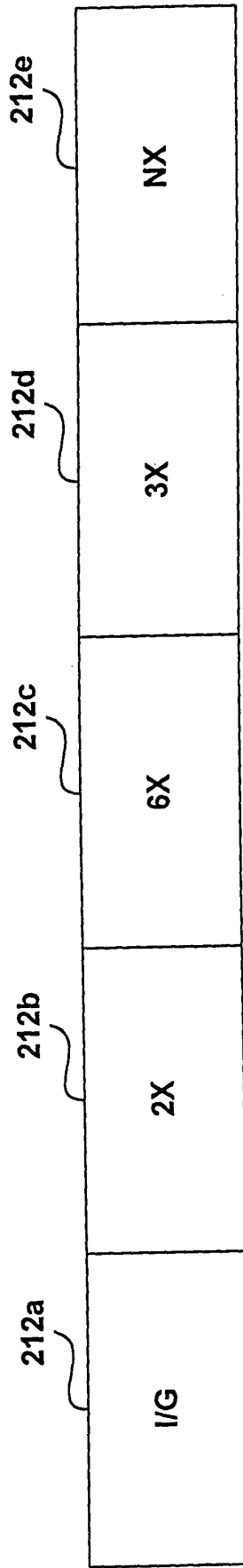


FIG. 2C

FIG. 2D is a schematic diagram of a system 204a, which includes a processor 212a, a memory 212b, a network interface 212c, a storage device 212d, and a user interface 212e.



204a

FIG. 2D

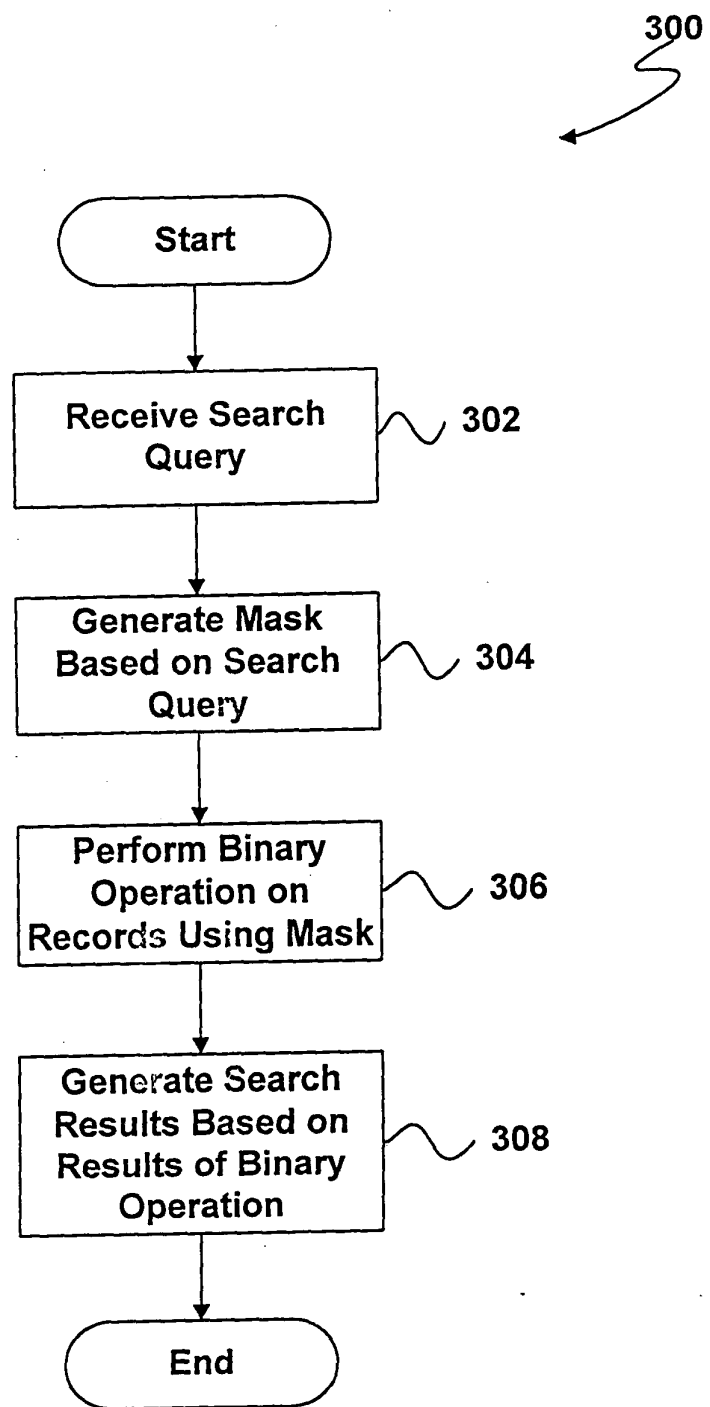


FIG. 3